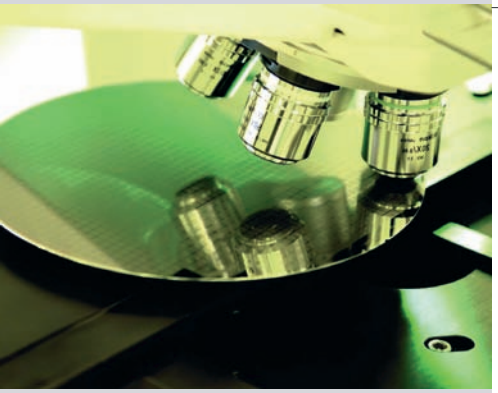
PROJECT RESULT

EDA for SOC Design and DFM

MEDEA+

2A713: Highly optimised design methods for yield and reliability (HONEY)



Faster circuit design for safety-critical applications

Increasing automation is pushing reliability to the fore in chip design and manufacture. In safety-critical areas such as fly-by-wire, collision-avoidance systems, radar and emergency communications, the consequences of circuit failure can be severe. Yet designing in sufficient redundancy to ensure 100% reliability is prohibitively expensive. The HONEY project has streamlined chip design and developed automated design methods to improve manufacturing yield. Statistical and systematic design methods at an early stage of circuit design speed up new chip generation and improve operational reliability.

Society expects ever higher levels of reliability from electronics. Safety-critical applications in transport, medicine and industrial production demand as close to 100% reliability as possible, or the redundancy to allow for any failures. This is no easy matter when even a mid-priced car can contain up to 80 networked electronic systems and some 1,000 chips. And, as the number of safety, environmental control and comfort applications grow, these numbers are set to increase.

Existing systems have to be smaller and new ones as compact as possible. Yet the push for ever higher levels of chip integration to reduce both size and power consumption is revealing new integrated-circuit behavioural phenomena which detract from manufacturing yield and longer-term circuit reliability. The MEDEA+ 2A713 HONEY project therefore set out to research these phenomena and develop automated methods for the design process that could help predict them, or circumvent likely problems.

Focus on yield and reliability

The main focus for HONEY was the ramp-up stage in the chip-production process from low volume – and low yield – to full-scale commercial production. The main objective was to address the issue of yield without affecting the silicon process. However the project also took into account circuit compliance with specifications over the full operational life as a better understanding of manufacturing-yield and operational-reliability issues results in an improved design-flow process.

HONEY focused on analogue and mixed-signal circuits in the 350 to 90 nm CMOS/BiCMOS area used in many automotive and industrial applications, as well as targeting the 90 to 32 nm CMOS nodes more common in the communications sector. In total, the project addressed some nine chip-design nodes.

Phase 1 examined software tools and models at prototype level, then developed the first test chips with a focus on the 65 nm node. Phase 2 improved predictions and optimisations from Phase 1 while focusing on the 45 nm node. This phase also saw the development of an exploitable toolbox – including software tools and models – for use by the partners. Phase 3 extended the sets of models developed to take into consideration the 40 to 28 nm nodes and beyond.

At the methodology level, the main innovation was to move design-for-manufacturing upstream in the design process, creating designs that would be problem-free during manufacture as well as reliable in operation. By the end, the project had produced models and a toolkit – software tools and monitoring structures – extending from the hardware-

development level through place-and-route down to the layout level.

Improvements to automation of the design flow included yield prediction, electromigration robustness evaluation, critical-area analysis, layout generation, layout improvement – hot-spot repair and correction of library models – and generation of monitoring structures.

Saving design time

Yield evolution is a particularly important factor in helping silicon manufacturers to be fast to market. HONEY results have enabled the project partners to accelerate the learning speed at the 45 nm node by about 50% in comparison with 65 nm. This means that learning – that is reaching a significant yield increase – can now be performed in six months rather than a year. Such a gain can lead to savings of more than €70 million per month.

HONEY results have helped the partners save in the design area by reducing mismatch validation time by 75%, developing more efficient methods of reusing existing layouts and gaining up to a 30% saving in time over traditional design experimentation.

Partners were also able to increase yield, for example by minimising losses from wire spreading or wire fattening. In random yield, a reduction in safety margins has led to a better trade-off between yield/reliability and performance, while a reduction in chip area has had an immediate impact in terms of cost – for example a 60% area reduction with no loss of analogue circuit performance demonstrated on a BiCMOS silicon chip.

Results being applied

The results of this MEDEA+ project are already being exploited in the design of safety-critical applications. For example new library-certification software in terms of yield and reliability has been developed for the automotive sector that is fully certified by and for the industry.

Car-safety applications comprise around 14% of the total automotive semiconductor market. They are estimated to be worth over €2 billion in 2012, and are showing a growth rate of 17% a year for safety-critical chips – 4% more than the growth in the total automotive semiconductor market. Less critical but still high-volume, automotive-entertainment applications are already using the library yield system developed in HONEY.

In the telecommunications field, a new assessment method for standard library cells has been developed in the 65/40 nm libraries for fixed-line applications. Baseband circuits have been used as demonstrators to show process-yield monitoring and reliability profiles.

There were also knowledge transfers from the two participating research organisations to the industrial partners. The design methods developed in HONEY will be put to use by more than 20 European design centres, and will benefit six European chip-production centres.

HONEY has produced a total of some 52 research papers. The last year of the project was particularly productive, with 27 papers published or submitted in 2010. A doctoral thesis closely linked to the work on soft breakdown performed in HONEY was also defended in 2011.

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